Innoscience 英诺赛科

POWER THE FUTURE

AN002

Application Note

LV InnoGaN

Gate Driving Design Guide

List of Content

1. Introduction of InnoGaN Gate Driving Characteristics

1.1. InnoGaN structures

Figure 1 shows the structure of InnoGaN. InnoGaN is a power device with p-GaN enhanced gate (e-mode). When the built-in positive voltage generated by the charge of the p-GaN structure is higher than the voltage generated by the AlGaN/GaN hetero-junction, it will deplete the 2DEG underneath the gate to form an enhancement device. P-GaN structure can be regarded as a Schottky and a PN junction connected back to back in series. This structure limits the gate-to-source voltage rating. The max gate-to-source voltage for current LV InnoGaN products is 5.5V/6V. Please refer to the corresponding datasheets for more information.

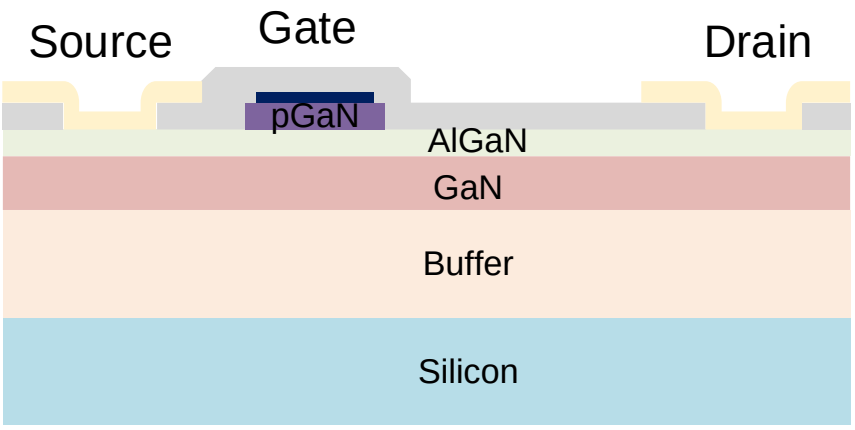


Figure 1 p-GaN enhanced GaN FET structures

1.2. Low-voltage InnoGaN gate characteristics

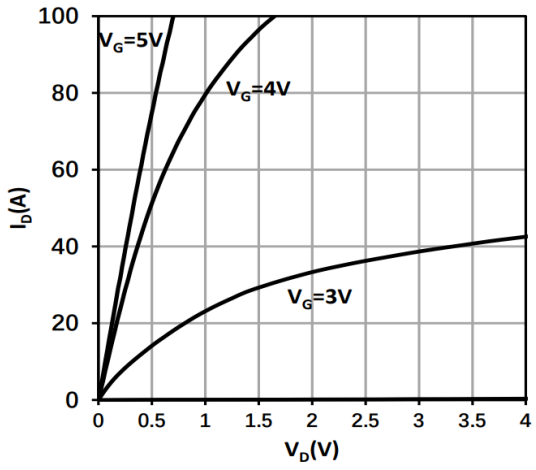
Limited by the p-GaN structure characteristics, the max positive GS voltage rating is 5.5V/6V, while negative GS voltage rating is -4V, In the design process, attentions should be paid to the selection of driving voltage and layout design, to avoid gate over-voltage.

Table 1 Key Characteristics of LV InnoGaN

Symbol	Parameter	Max.	Unit
V_{DS}	Drain-to-Source Voltage（Continuous）	100	V
I_D	Continuous current	60	A
	Pulsed（25℃, TPULSE = 300 us）	230	A
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
T_J	Operating Temperature	-40 to 150	℃
T_{STG}	Storage Temperature	-40 to 150	℃

The following figure shows the Vgs-Id curve and Vgs-Rdson curve of the INN100W032A product as an example. In practical applications, it is recommended that the high-level GS voltage should be high enough, so that the GaN FET is fully enhanced r and performs higher current capacity and efficiency.For current low-voltage InnoGaN products, the recommended high-level GS voltage is 5V.

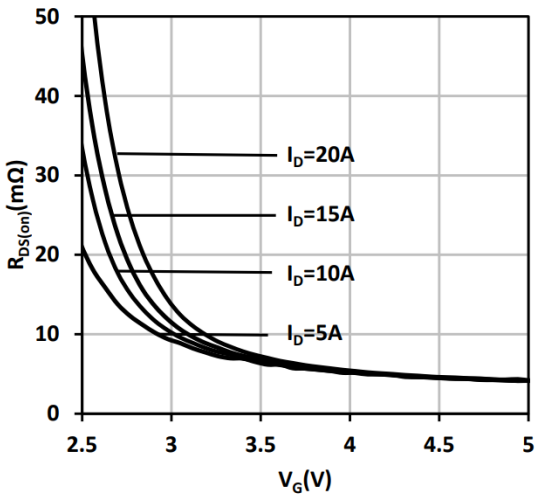
Figure 1 Typical Output Characteristics



$I_D = f(V_D, V_G)$; T_J = 25 °C

Figure 2 Vgs-Id curve

Figure 3 Typical Drain On-state Resistance



$R_{D(on)} = f(V_G, I_D)$; T_J = 25 °C

Figure 3 Vgs-Rdson curve

1.3. Comparison of e-mode GaN FETs and Si MOSFETs

- **Similarities:**

1、 E-mode GaN FETs and Si MOSFETs are both normally-off power devices.

2、 Voltage- driven: During the switching process, the drive voltage charges and discharges the parasitic capacitance Ciss/Crss of the deivce, and provides gate leakage current Igss with positive bias.

3、 Switching speed could be modeified by external gate resistance Rg_ext.

- **Difference:**

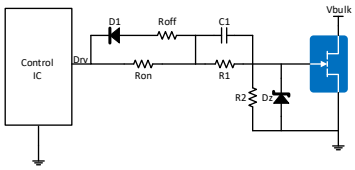
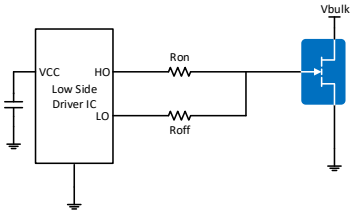
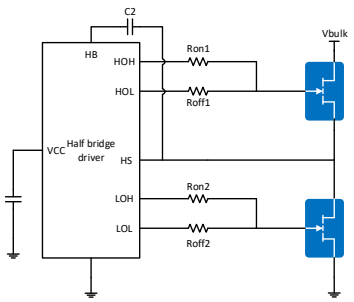
1、 Gate voltage rating and Vth threshold are lower, requiring careful handling of the driving circuit to avoid ringing leading to fault turn-on/off.

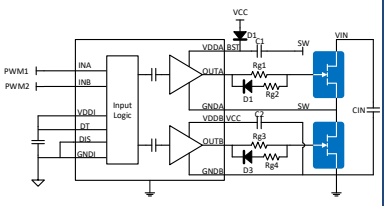
2、 The recommended driving voltage of low-voltage InnoGaN FET is 5V, which is lower than the 8~12V driving voltage for Si MOSFET. To be compatible with the controller that are designed for Si MOSFET, voltage divider or additional gate drivers are necessary to adapt the gate voltage requirement of LV InnoGaN.

3、 InnoGaNshas lower Ciss, Crss, lower driving losses, and faster switching speed.

2. Categories of LV InnoGaN Gate Driving Circuits

Table 2 Categories of LV InnoGaN Gate Driving Circuits

Categorization			Schema	Specificities	Applicable Scenarios
Single	Non-isolated	voltage-divider		Compatible with controllers and driver IC with voltage higher than 5.5V, adjustable driving voltage	Applications: Low Power Modules Topologies: Flyback
		Direct-driving		Simple driving circuits for high reliability and simpler driving loop design	Applications: Lidar、Low Power Modules Topologies : Flyback 、single switch
Half-bridge	non-isolated	direct-driving		Simple driving circuit optimized specifically for GaN devices, high reliability and simpler driving loop design	Applications: power modules, in-car fast charger, notebooks , data center, MHEV, Class D, Topologies : Buck、Boost、Buck-Boost、full-bridge、half-bridge、LLC

	Isolated	Integrated digital isolators and drivers		integrated isolated GaN drivers, with specifically optimized for the driver for high reliability	Field: Power Modules Topologies : full-bridge、 half-bridge、LLC

3. Single-GaN gate Driving Design

3.1. Voltage Divider Gate Driving

3.1.1. Circuit Diagrams

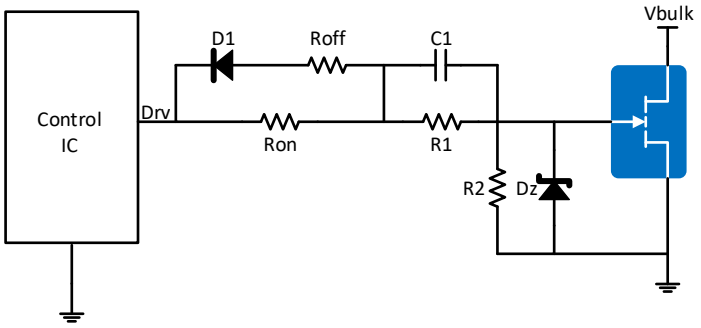


Figure 4 Voltage divider driving circuit

3.1.2. Functions of Components in Voltage Divider Driving Circuits

Table 3 Functions of Components in Voltage Divider Driving Circuits

Electronic component	Functions
Ron	Modify the turn-on speed of GaN FET
Roff	Modify the turn-off speed of GaN FET
Z1	Clamping the Gate voltage of GaN FET
R1	Voltage dividing resistors
R2	
C1	Switching Acceleration Capacitor

3.1.3. Switching Process with Voltage Divider Gate Driving Circuits

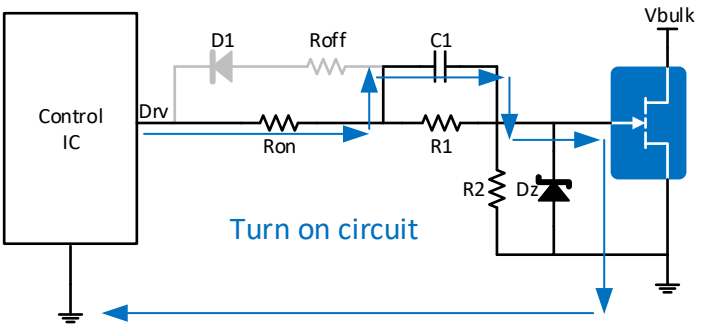


Figure 5 Turn-on loop of voltage dividing driving circuit

The turn-on loop is shown in Figure 5. VDRV charges Ciss of the GaN FET through Ronand C1, making Vgs voltage rises rapidly thus turning on the GaN Device.

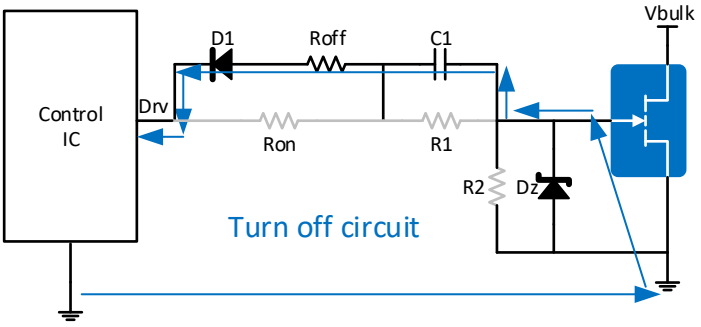


Figure 6 Turn-off loop of voltage dividing driving circuit

During the turn-off process, the gate driving current flow is shown in Figure 6. VDrv discharges the Ciss/Crss of high-voltage InnoGaN rapidly through D1, Roff, and Cc, causing the Vgs voltage to decrease quickly, thus turning off the power transistor An design example of the parameters in voltage divider driving circuit:

High-level Voltage of Si Driver IC: DRV = 10V

Driving Voltage of GaN: Vgs = 5V

Igss of GaN @125℃: Igssmax = 500μA

GS Parallel Resistor: R2 = 10kΩ

Sum of R1 and Ron: Rtotal = $\frac{DRV-Vgs}{\frac{Vgs}{R2}+Igssmax}$ = 5kΩ

Ciss = 805pF Qg = 6.2nC

Minimum acceleration capacitance: C1 = $\frac{Qg}{DRV-Vgs}$ = 1.24nC

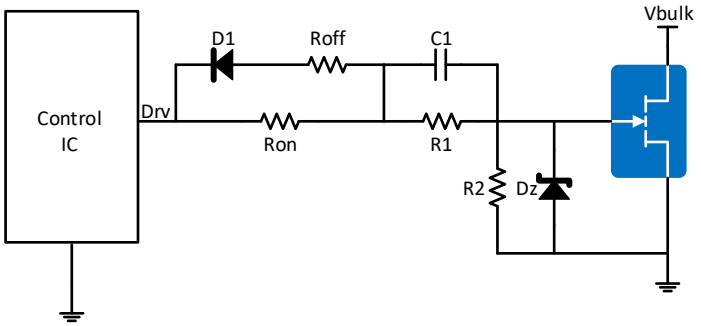


Figure 7 Parameter calculation of voltage dividing driving circuit

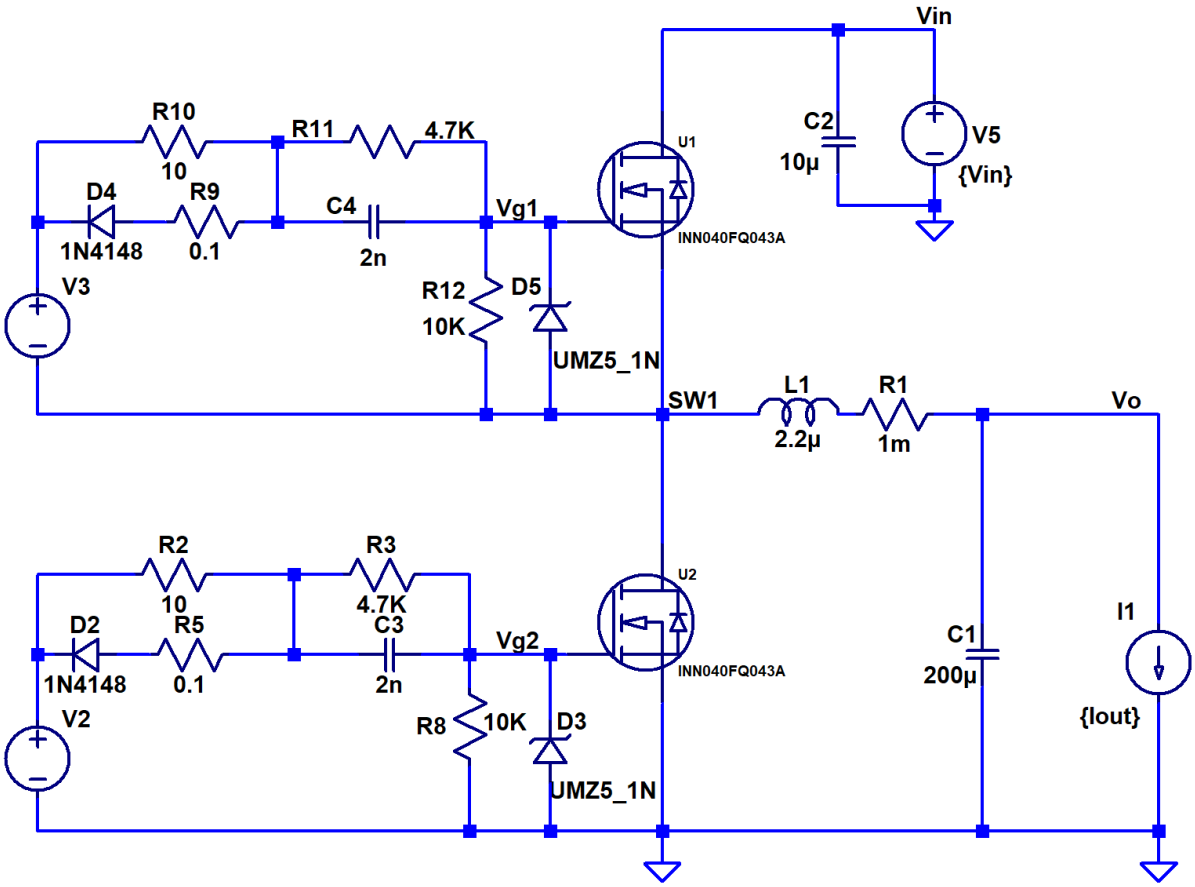


Figure 8 Simulation Circuit Diagram

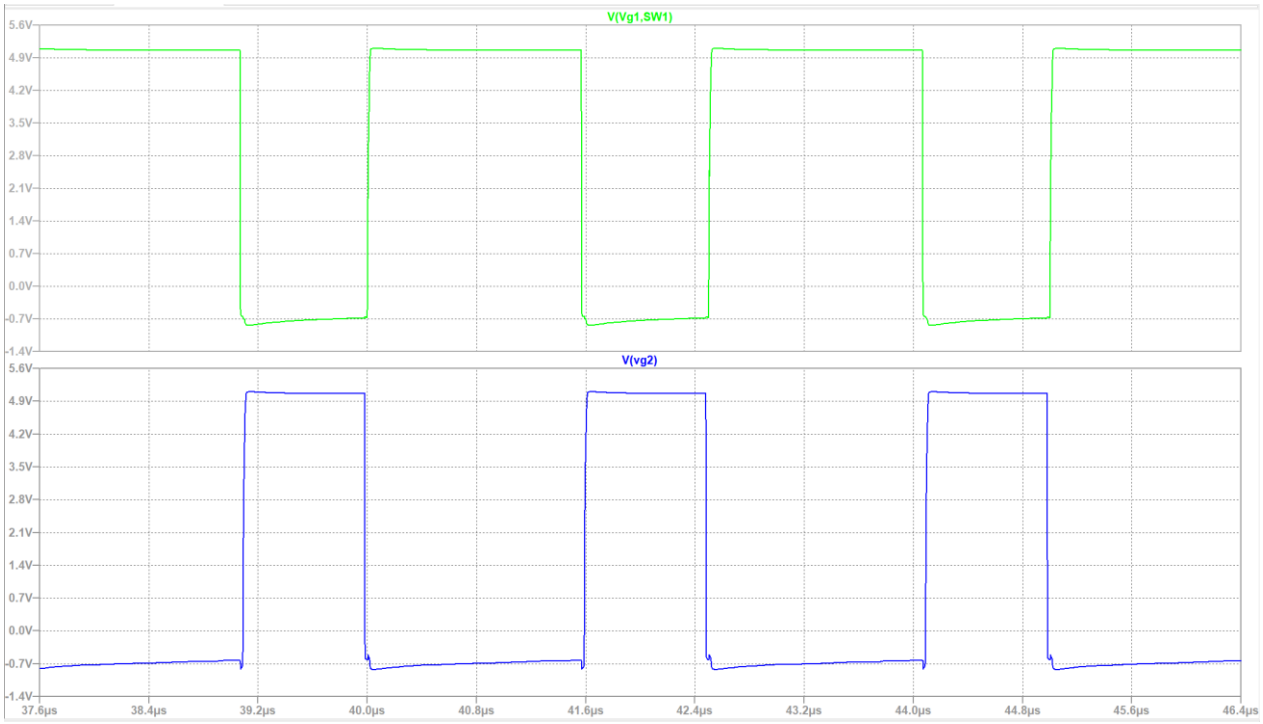


Figure 9 Simulation Waveforms

3.1.4. Voltage Divider Design Considerations

3.1.4.1.Driving voltage of the controller

The driving voltage varies from different controllers. So the voltage dividing resistor should be adjusted to match the appropriate GaN FET driving voltage. The recommended driving voltage is 5V, while the maximum voltage should be under 6V. Vgs is calculated as follows:

$$\mathrm{R1} + \mathrm{Ron} = \frac{Vdrv - Vgs}{\frac{Vgs}{R2} + Igssmax}$$

Where Vdrv is the driving voltage of the controller, R1, R2 is the voltage dividing resistor, and the recommended resistance of R2 is 10kΩ.

3.1.4.2.Effect of C1 capacitance on driving

The resistance of the voltage divider is relatively high, resulting in very low driving current during the switching process and low speed switching of GaN FETs., With the low AC impedance of the capacitor C1, which is connected in parallel with R1, most of the current flows through C1 to charge and discharge the Ciss of GaN FETs during the switching processes and thus achieve fast switching. During the switching processes, C1 and Ciss are in series, and the charge of C1 must be greater than Ciss to ensure rapid charging and discharging of Ciss to effectively turn-on and turn-off the LV InnoGaNs, satisfying the following equation:

$$\mathrm{C1} \gg \frac{Qg}{Vdrv - Vgs}$$

The impact of different capacitance on the driving waveforms are shown in Figure 10, . A too small C1 will lead to slower switching speed with a risk of not being able to turn on or turn off the deivce in time. Given that Cc meets the requirements, a larger Cc results in a longer negative gate-source voltage duration during off time.

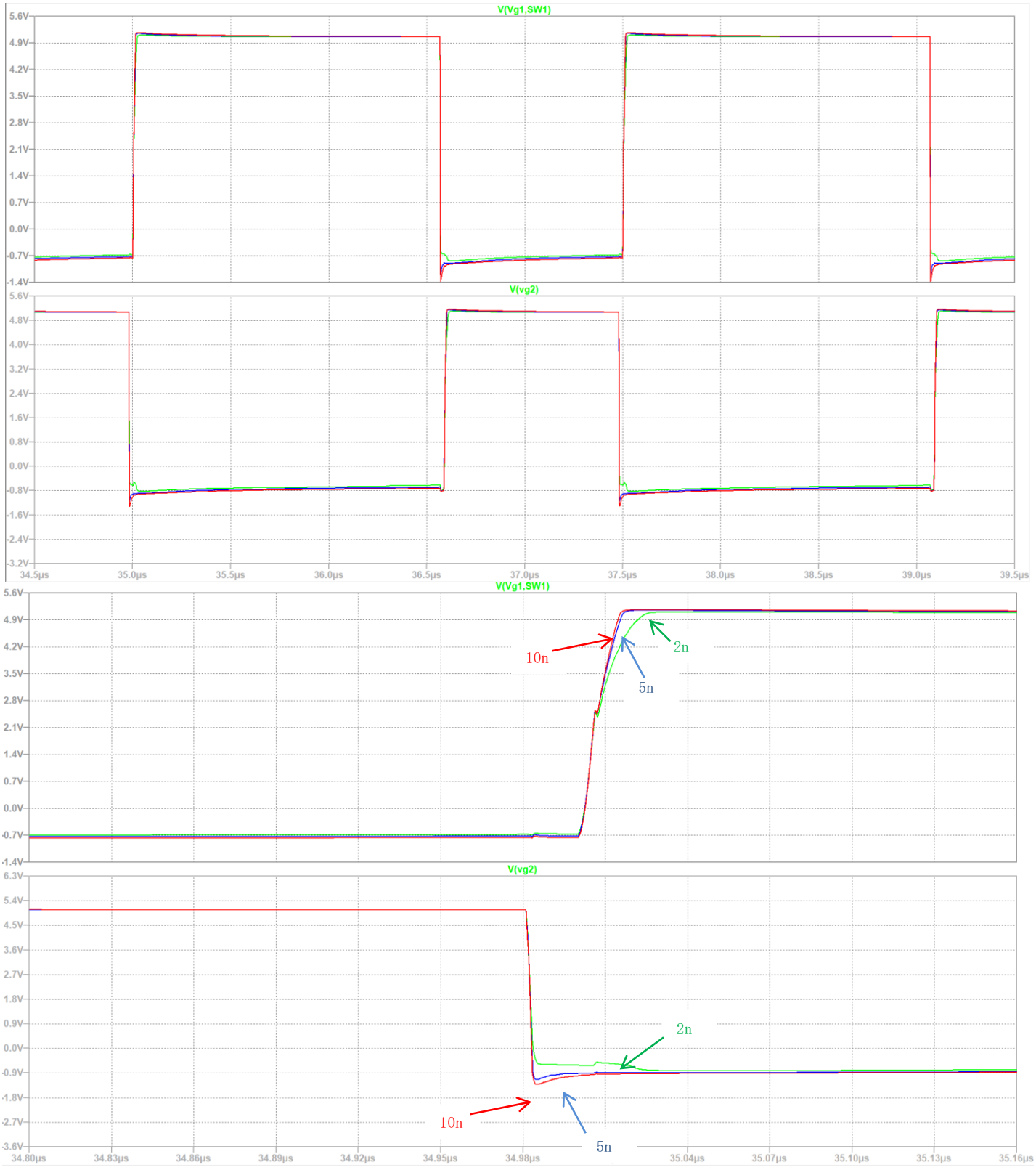


Figure 10 Effect of different capacitance values on driving waveforms

3.1.4.3.Selection of Zener Diodes

The main function of the zener diode is to clamp thegate-source voltage of the GaN FET within specifications to ensure the gate reliability. It is recommended to use a 5.1V zener diode with the max value of less than 6V.

Table 4 Voltage regulator diode selection

Device*	Device Marking	V_{Z1} (V) @ I_{ZT1} = 5 mA: 2.4 to 24 V I_{ZT1} = 2 mA: 27 to 75 V (Note 1)			V_{Z2} (V) @ I_{ZT2} = 1 mA (Note 1)		Zener Impedance			Leakage Current		ΘV_Z (mV/k) @ I_{ZT}		C @ V_R = 0 f = 1 MHz
							Z_{ZT} @ I_{ZT}	Z_{ZK} @ I_{ZK}		I_R @ V_R				
		Min	Nom	Max	Min	Max	Ω	Ω	mA	μA	Volts	Min	Max	pF
MM5Z2V4T1G	00	2.2	2.4	2.6	1.7	2.1	100	1000	1.0	50	1.0	−3.5	0	450
MM5Z2V7T1G	01	2.5	2.7	2.9	1.9	2.4	100	1000	1.0	20	1.0	−3.5	0	450
MM5Z3V0T1G	02	2.8	3.0	3.2	2.1	2.7	100	1000	1.0	10	1.0	−3.5	0	450
MM5Z3V3T1G	05	3.1	3.3	3.5	2.3	2.9	95	1000	1.0	5	1.0	−3.5	0	450
MM5Z3V6T1G	06	3.4	3.6	3.8	2.7	3.3	90	1000	1.0	5	1.0	−3.5	0	450
MM5Z3V9T1G	AJ	3.7	3.9	4.2	2.9	3.5	90	1000	1.0	3	1.0	−3.5	0	450
MM5Z4V3T1G	08	4.0	4.3	4.6	3.3	4	90	1000	1.0	3	1.0	−3.5	0	450
MM5Z4V7T1G	09	4.4	4.7	5.0	3.7	4.7	80	800	1.0	3	2.0	−3.5	0.2	260
MM5Z5V1T1G	0A	4.8	5.1	5.4	4.2	5.3	60	500	1.0	2	2.0	−2.7	1.2	225
MM5Z5V6T1G	0C	5.2	5.6	6.0	4.8	6	40	200	1.0	1	2.0	−2.0	2.5	200

3.2. Direct-driving

3.2.1. Direct-Driving Circuit

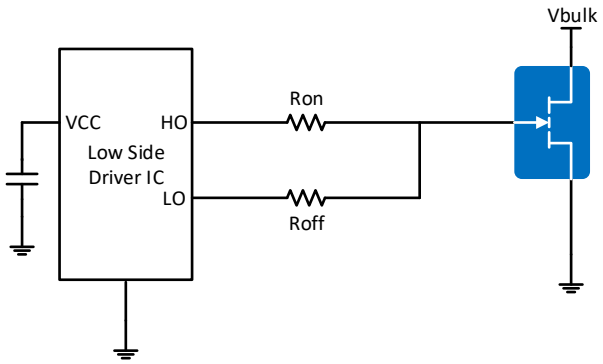


Figure 11 Direct Driving Circuit

3.2.2. Functions of each components in the direct-driving circuit

Table 5 Functions of each components in the direct-driving circuit

Electronic component	Functions
Ron	Modify the turn-on speed of GaN FET
Roff	Modify the turn-off speed of GaN FET

3.2.3. Switching Processes of Direct-driving Circuits

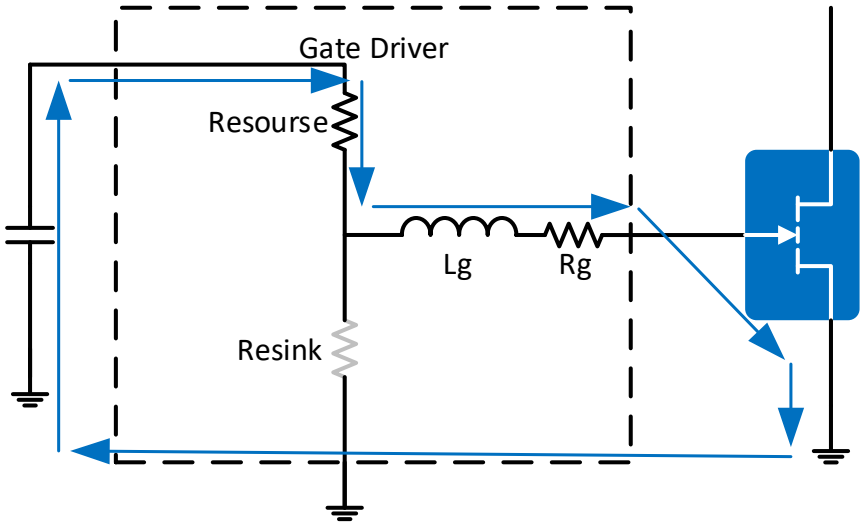


Figure 12 Turn-on loop of direct driving

The turn-on loop is shown in Figure 12, The current flows from the positive side of the VCC capacitor, through the chip built-in pull-up resistor Rsource parasitic inductance Lg, gate resistor Rg, and to the Gate terminal of the GaN FETs, then flows through the Source terminal of the GaN FETs back to the negative end of the VCC capacitor.

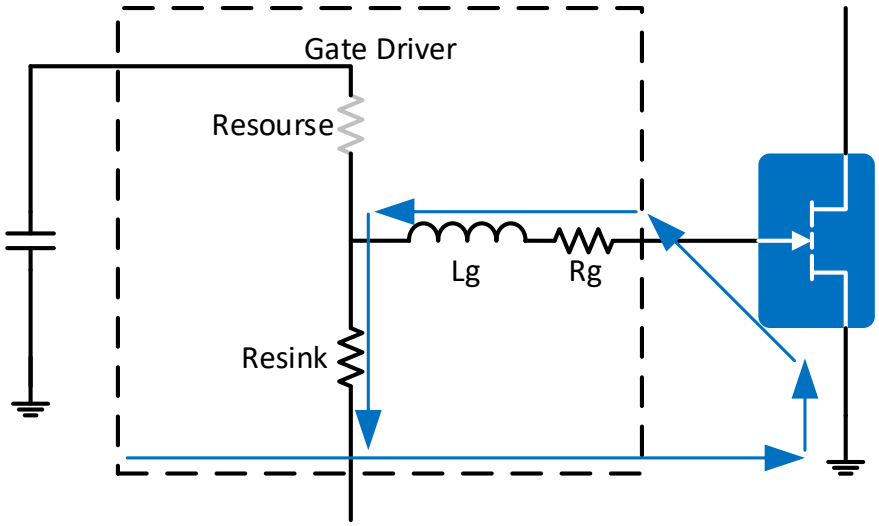


Figure 13 Turn-off loop of direct driving

The turn-off process, driven by the current loop as shown in Figure 12, Gate discharging current flows through Rg, Lg, Rsink, to GND.

3.2.4. Example of direct-driving circuit design

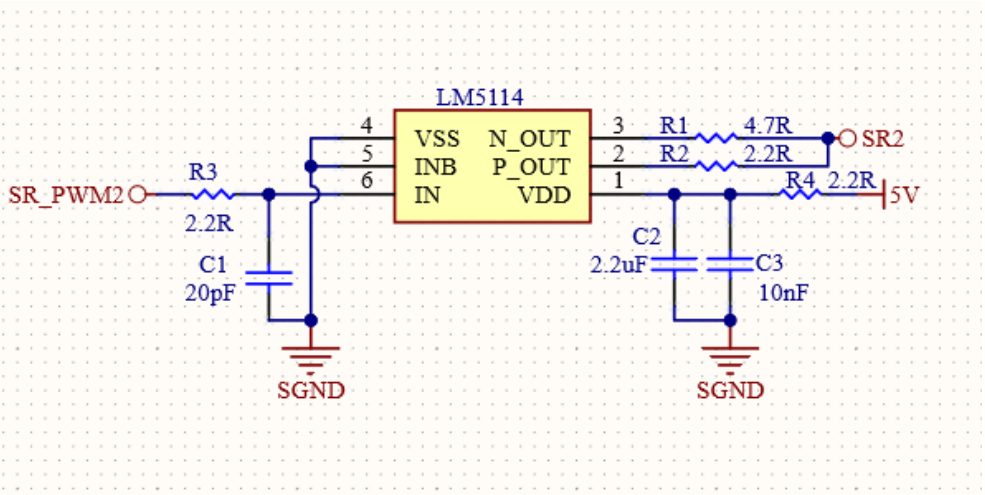


Figure 14 Example of direct -driving circuit design

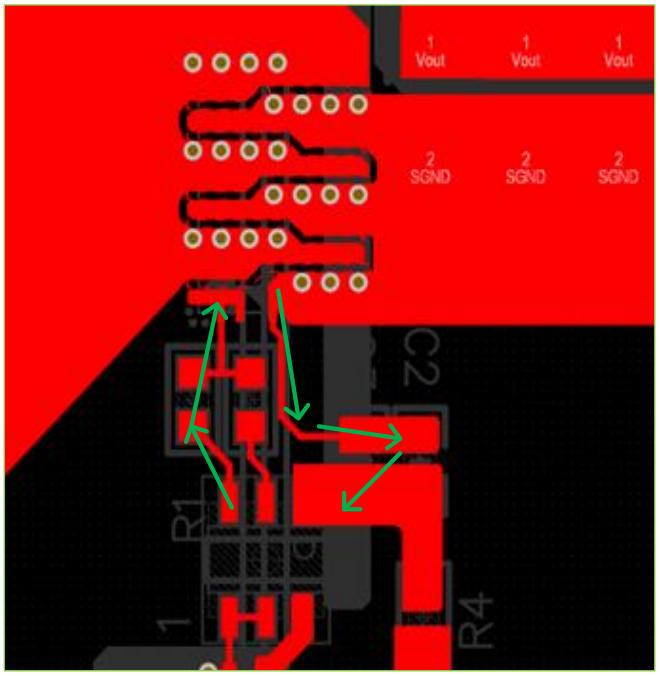


Figure 15 Direct Driving Circuit Layout Design Example

3.2.5. Considerations for Direct-Driving

1、 VCC decoupling capacitor should be close to the driver IC to reduce the ringing in the gate driving loop;

2、 To reduce the loop inductance, the driver should be as close as possible to the GaN to reduce parasitic inductance in the loop;

3、 Reduce the common source inductance to minimize the coupling between the driving and the power loop ;

3.2.6. Direct driving IC Recommendation

Table 6 Recommended Direct Drive IC

Part Number	Manufacturer	Pulldown resistance/Pullup resistance（Ω）	Peak source current/Peak sink current (A)	Propagation Times(ns)	Split outputs	Application
LM5114	Texas Instruments	2/0.23	7.6/1.3	12	Y	Universal single GaN low-side gate driver
LMG1020	Texas Instruments	-	7/5	2.5	Y	GaN low-side gate driver for high-speed, high-frequency applications up to 60MHz with a minimum pulse width of 1ns
uP1964	uPI Semiconductor	2/0.5	5.5/2	30	Y	Universal single GaN low-side gate driver

4. Half-bridge Gate Driving Design

4.1. Half Bridge Non-Isolated Driving

4.1.1. Half Bridge Non-Isolated Driving Circuit

The half-bridge non-isolated driver is suitable for topologies such as LLC, Buck, Boost, etc. The application block diagram is shown as follows:

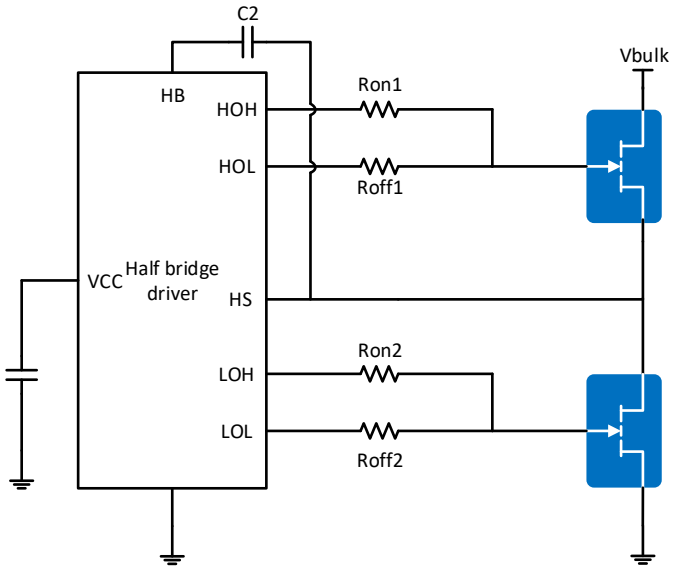


Figure 16 Half Bridge Non-Isolated Driving Circuit

4.1.2. Function of Each Components H

Table 7 Function of Each Components in galf-bridge non-isolated driving circuit

Component	Functions
Ron	Modify turn-on speed of GaN FETs
Roff	Modify turn-off speed of GaN FETs

4.1.3. Switching process of half-bridge non-isolated driving

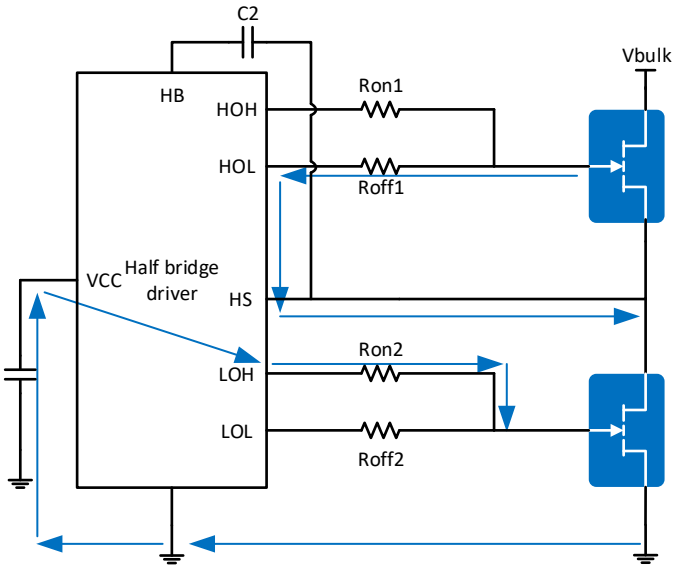


Figure 17 Low side turn-on process

The current flow in low side turn-on/ high side turn-off process is shown in Figure 17. The driving current flows from the positive side of the VCC capacitor through LOH pin of the driver IC and Ron2 to the Gate of the GaN FET, then flows through the Source of the GaN FET back to the negative side of the VCC capacitor. In this process, the mid-point voltage of the half-bridge is at low level thus on the bootstrap capacitor of high side GaN FET is charged. In the turn-on process of the high side GaN FET, the driving current flows from the Gate of high side GaN FET through Roff1, the HOL pin of the driver, then from HS pin of the driver to the mid-point of the half-bridge.

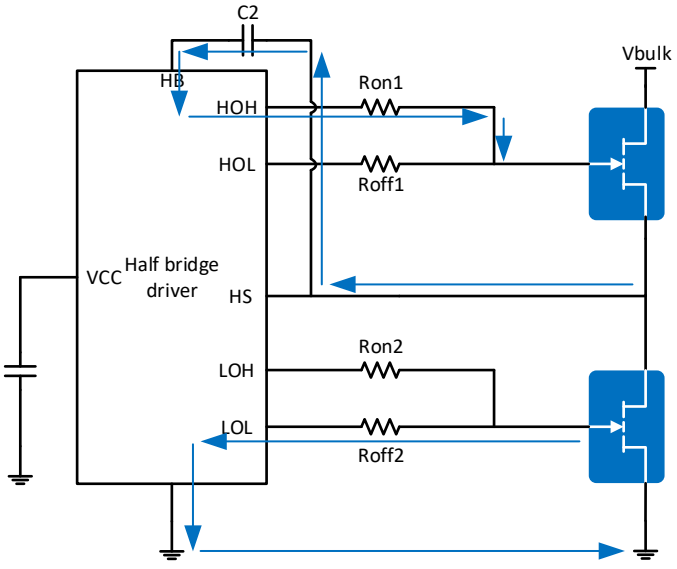


Figure 18 High side turn-on process

The current flow in high side turn-on/ low side turn-off process is shown in Figure 18. The driving current of high side GaN FET flows from the positive side of capacitor C2 , through the HOH pin of the driver, Ron1, and then to the Gate of GaN FET. thenflows back through the Source of GaN FET to the HS point. In the turn-off process of the low side GaN FET, the driving current flows from the Gate of low side device through Roff2, LOL pin of the driver to GND.

4.1.4. Design Example of Half-bridge non-isolated Driving Circuit

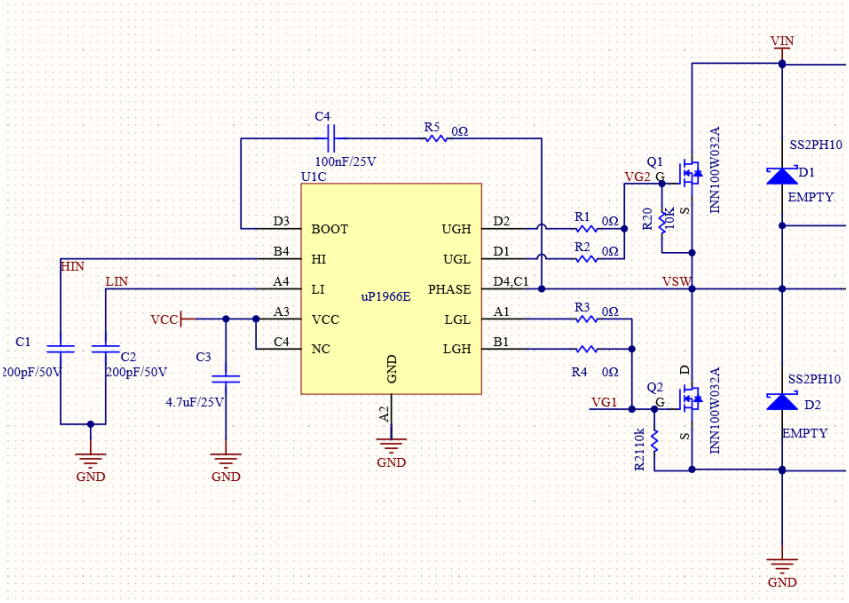


Figure 19 Design example half-bridge non-isolated driving circuit

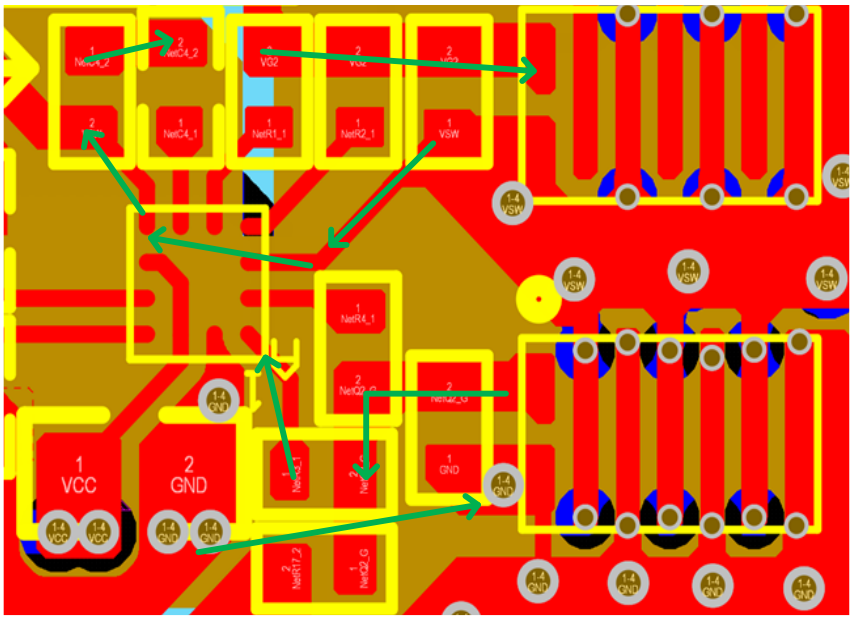


Figure 20 Layout Design Example of Half Bridge Non-Isolated Driving Circuit

4.1.5. Design Considerations of Half Bridge Non-Isolated Driving Circuit

1、 VCC decoupling capacitor should be close to the driver IC pins to minimize ;

2、 Place the driver IC as close as possible to the GaN to minimize the loop parasitic inductance;

3、 Reduces coupling between drive and power circuits and reduces common-source inductance;

4、 Bootstrap capacitors should be close to the driver IC pins, and avoid the overlap between the gate driving loop and the power loop to reduce the impact of the power circuit dV/dt on the driving circuits ;

4.1.6. Recommended Half Bridge Non-Isolated Driving ICs

Table 8 Recommended Half Bridge Non-Isolated Driving ICs

Part Number	Manufacturer	Max voltage(V)	Peak source current/Peak sink current (A)	Propagation Times(ns)	Max Frequency	Application
LMG1210	Texas Instruments	200	3/1.5	10	50MHz	Ultra-high frequency half-bridge driver supporting 200V input for GaN
LM5113-Q1	Texas Instruments	100	5/1.2	1.5	-	Half bridge gate drivers that meet automotive standards
LMG1205	Texas Instruments	100	5/1.2	1.5	-	A universal GaN half-bridge driver that supports 100V input
uP1966A	uPI Semiconductor	80	-	20	-	A universal GaN half-bridge driver that supports 100V input
MPQ1918	MPS	100	4/2	1.5	4	High-side floating bias voltage rail operates up to 100 VDC

4.2. Half Bridge Isolated Driving Circuit Design

4.2.1. Half Bridge Isolated Driving Circuit

In power supply applications with isolation requirements, such as hard-switching full-bridge, phase-shift full-bridge and other topologies, the primary and secondary sides need to be isolated to meet the voltage withstand requirements. Thus the PWM signals and the gate driving signals need to be isolated. The block diagram of isolated half-bridge driving circuit is shown as below.

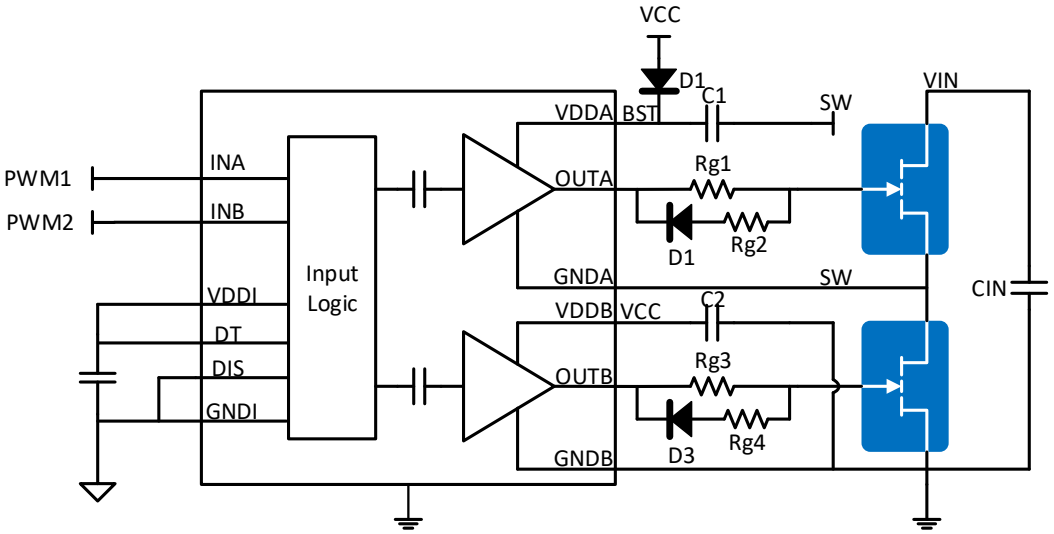


Figure 21 Integrated digital isolation and driver in half-bridge driving circuit

4.2.2. Switching Process of Half-bridge Isolated Driving Circuit

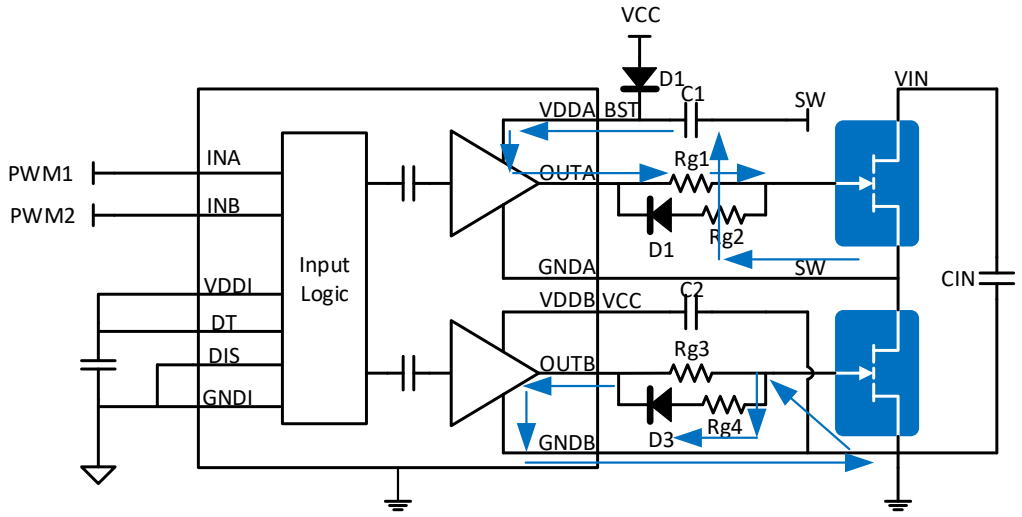


Figure 22 High side Turn-On Process of Half Bridge Isolated Driving Circuit

The current flow in low side turn-on/ high side turn-off process is shown in Figure 22. The driving current flows from the positive side of the C1 capacitor through OUTA pin of the driver IC and Rg1 to the Gate of the GaN FET, then flows through the Source of the GaN FET back to the negative side of the C1 capacitor. In the turn-off process of the low side GaN FET, the driving current flows from the Gate of high side GaN FET through Rg4,D3 to the OUTB pin of the driver, then to GND.

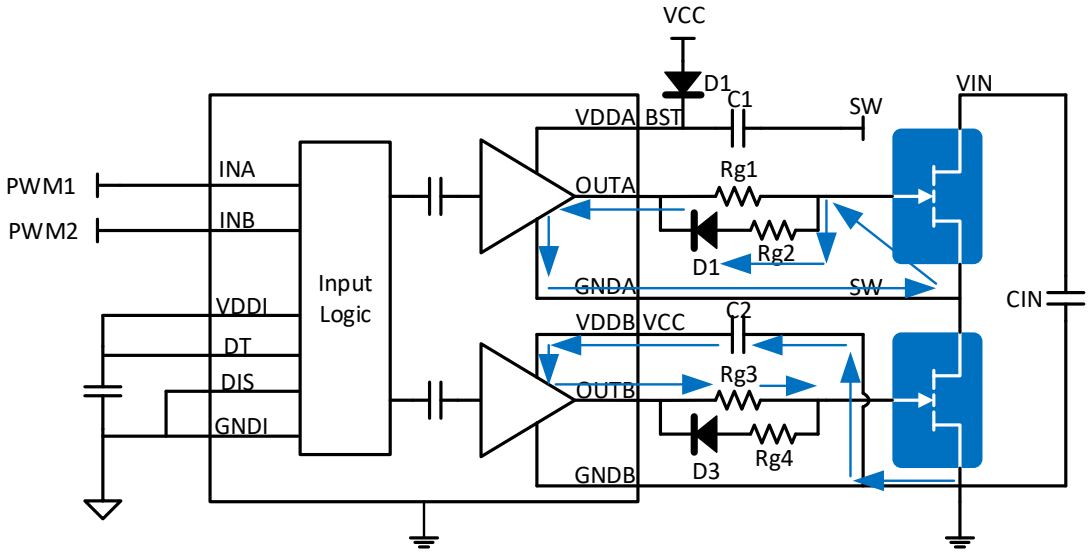


Figure 23 Low side turn-off process of half-bridge isolated driving

The current flow in low side turn-on/ high side turn-off process is shown in Figure 23. The driving current flows from the positive side of the capacitor C2 through OUTB pin of the driver IC and Rg3 to the Gate of the GaN FET, then flows through the Source of the GaN FET back to the negative side of C2. In this process, the mid-point voltage of the half-bridge is at low level thus on the bootstrap capacitor of high side GaN FET is charged. In the turn-off process of the high side GaN FET, the driving current flows from the Gate of high side GaN FET through Rg2, D2, the OUTA pin of the driver, then from HS pin of the driver to the mid-point of the half-bridge.

4.2.3. Design Example of Half Bridge Isolated Driving Circuit

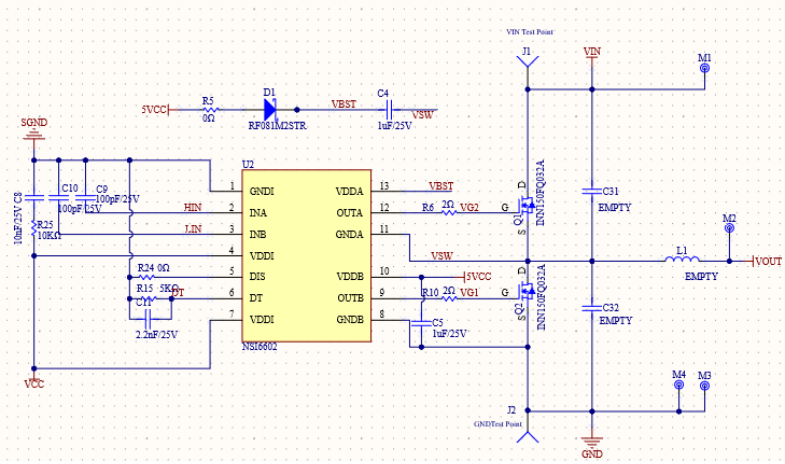


Figure 24 Design Example of Half Bridge Isolated Driving Circuit

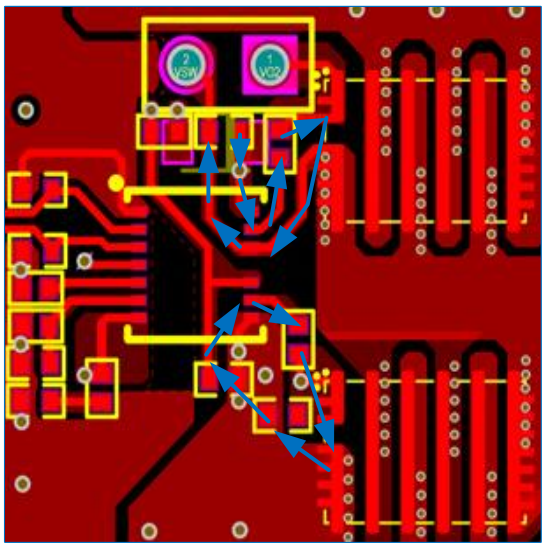


Figure 25 Half Bridge Isolated Driver Circuit Layout Design Example

4.2.4. Design Considerations of Half Bridge Isolated Driving Circuits

1、 Low ESR and low ESL bypass capacitors should be placed close to the VCC pins of the driver ICs , such as between VDDI-GND, VDDA-GNDA, and VDDB-GNDB.

2、 The isolated driver should be placed close to GaN FETs to reduce the driving loop area and ringing problems and optimize EMI performance.

3、 Reduce common source inductance to avoid high di/dt issue that affect the switching actions of GaN FETs.

4.2.5. Recommendation of Half Bridge Isolated Driver ICs

Table 9 Recommendation of Half Bridge Isolated Driver ICs

Part Number	Manufacturer	Peak source current/Peak sink current（A）	Propagation Times(ns)	Application
NSI6602EA	Novosense	6/8	25	NSI6602E is a high-reliability dual channel isolated gate driver that could be designed in a variety of switching power and motor drive topologies
Si8273	SILICON LABS	1.8/4	60	Si8273 controlled using the VIA and VIB input signals
Si8274	SILICON LABS	1.8/4	60	Si8274 controlled by a single PWM signal
UCC21550	Texas Instruments	4/6	33	UCC21550x-Q1 has a programmable dead time and a wide temperature range Isolation-type dual-channel gate driver series

Revision History

Date	Versions	Description	Author
2024/4/12	1.0	First edition	AE Team

Note:
There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.
Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.

Reminder:
This product contains parts that are susceptible to electrostatic discharge (ESD). When using this product, be sure to follow antistatic procedures.

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